PCM-QUAD02

Two-Channel PCMCIA Quadrature Encoder Input Board

User's Guide

MEASUREMENT COMPUTING™

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1.0 INTRODUCTION

Thank you for purchasing a top quality PC data acquisition and control product from Measurement Computing Corporation. The PCM-QUAD02 is an 8-bit Type II PCMCIA card that provides inputs and decoding for up to two incremental quadrature encoders. The PCM-QUAD02 may also be used as a high speed pulse counter for general counting applications.

1.1 Quadrature Encoders and the PCM-QUAD02

Incremental quadrature encoders are used to provide feedback signals from motors, that is, to count rotations and convert the physical movement into a series of electrical signals. These signals are sent to the computer which then decides whether or not to trigger signals that control the motor's movement and what those control signals should be. The PCM-QUAD02 is the link between up to two incremental quadrature encoders and the computer.

The PCM-QUAD02 board is an 8-bit TYPE-II PCMCIA card that provides two channels for interfacing to incremental quadrature encoders. The heart of this product is the LS7266, a 24-bit dual-axis quadrature counter IC from LSI Computer Systems, Inc. This component contains:

- 24-bit counters
- Associated 24-bit preset and 24-bit output latch registers.
- Integrated digital filtering.
- 8-bit counter prescalers.
- programmable index functionality.
- programmable count modes including non-quadrature modes.

This functionality also enables the board to operate as a high speed pulse and general purpose counter, cascadable to 48 bits. The 24-bit counter can count either in binary or BCD through the CMR register.

The Phase A, Phase B, and Index inputs are factory-set prior to shipment for differential with termination resistor locations populated.

NOTES:

1. **If these resistor values are incorrect for your application, contact Measurement Computing Corporation to have them replaced.**

2. **Attempting to open the PCM-QUAD02 will void the warranty**.

Diagrams are supplied to show the user how to connect single-ended encoders to the card. These signals, after being routed through differential receivers, offer various paths to the LS7266 inputs. The inputs are routed through the FPGA to allow various configurations for:

- Individual encoder inputs for 2 channels.
- Cascadable counters to allow non-quadrature counting up to 48-bits.
- Routing of Index inputs to either the Load Counter/Load Latch input or the Reset Counter/Gate input with quarter-cycle and half-cycle supported.
- Routing the Compare or Carry/Borrow output signals to the interrupt circuit.

Also, you may generate interrupts from either the two Index inputs, counter overflow/underflow, or count value match. Two interrupt registers allow the software to enable/disable interrupts, mask individual interrupts, and read the source of the interrupt.

The incremental encoders connect to each channel through either a screw terminal board or user-configurable, non-terminated cable. The signals provided will be (per channel):

- Phase A+, A–
- Phase B+, B–
- Index+, Index–
- +5V and GND (optional power for 5V encoders, not to exceed 400mA peak)

For an overall view of how the PCM-QUAD02 is laid out logically (see Figure 1-1).

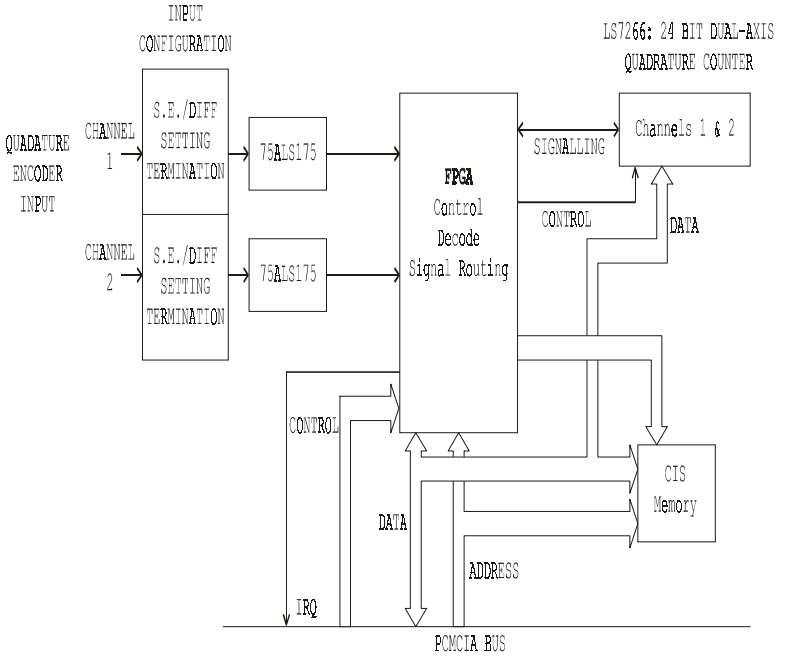

Figure 1-1. PCM-QUAD02 Block Diagram

2.0 SOFTWARE INSTALLATION

*Insta*Cal™ is the installation, calibration and test software supplied with your data acquisition / IO hardware. The complete *Insta*Cal package is also included with the Universal Library. If you have ordered the Universal Library, use the Universal Library disk set to install *Insta*Cal. The installation will create all required files and unpack the various pieces of compressed software. To install *Insta*Cal, refer to the *Extended Software Installation Manual* for complete instructions

3.0 HARDWARE INSTALLATION

The PCM-QUAD02 is completely plug-and-play. There are no switches or jumpers to set. Configuration is controlled by your system's PCMCIA Card and Socket Services. Simply insert the PCM-QUAD02 into any available PCM slot. Refer to Figure 2-1 for proper orientation of the card (the typical system orients the card with the label up).

Shown here is a PCM card case looking into the connector which is inserted into the PCMCIA slot of your computer. The key helps to insure that the PCM board is inserted correctly.

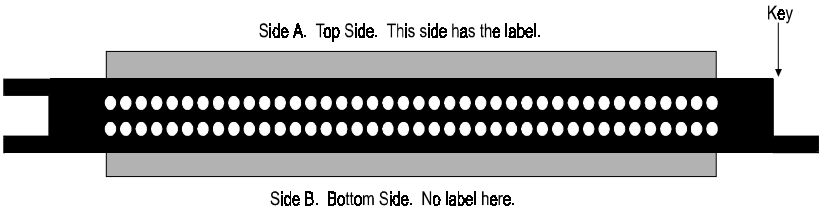

Figure 2-1. PCMCIA Card Orientation

If you are using an operating system with support for Plug and Play (such as Windows 95 or 98), a dialog box pops up on insertion of the card indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you are prompted for a disk containing it. The *Insta*Cal software that was supplied with your board (as well as the optional Universal Library software) contains this file. Just insert the disk or CD and click OK.

To easily test your installation, we recommend that you install InstaCal, the installation, calibration and test utility supplied with your board. Refer to the *Extended Software Installation Manual* for initial setup, loading, and installation of InstaCal and optional Universal Library software.

3.1 PCM-QUAD02 Ext. Connections, Input Configuration and Control

You can connect to the PCM-QUAD02 in one of two ways:
1. Use a standard AMP 15 pin I/O PCMCIA connector and non-terminated cable, such as Measurement Computing's PCM-C15-10-INCH.
(or)
2. Use a standard AMP 15 pin I/O PCMCIA connector with cable which is mated to a screw terminal board, such as the Measurement Computing's PCM-TERM15. See a recent Measurement Computing catalog for descriptions and pricing for these parts.
Pin assignments for both single-ended and differential connections are described below.

NOTE: **Be sure to properly phase the encoder according to the manufacturer's instructions.**

PIN ASSIGNMENTS

(AMP 15 position I/O connector):

Pin #	**Function**	**Pin #**	**Function**
1	Phase 1A+	9	+5VDC
2	Phase 1A–	10	Phase 2A+
3	Phase 1B+	11	Phase 2A–
4	Phase 1B–	12	Phase 2B+
5	Index 1+	13	Phase 2B–
6	Index 1–	14	Index 1+
7	Ground	15	Index 1–
8	+5VDC		

ENCODER INPUT

Termination: (footprints provided only)

	Resistors	
Input	Ch 1	Ch 2
Phase A	R1,2	R7,8
Phase B	R3,4	R9,10
Index	R5,6	R11,12

Differential Configuration: Default shown here for Phase A signals. Same exists for Phase B and Index.

15 pin PCMCIA Connector		Encoder
Phase 1A+	<----------	A+
Phase 1A-	<----------	A-

Single-Ended Configuration (shown here in Figure 3-2 for Phase A signals, same connections for Phase B and Index)

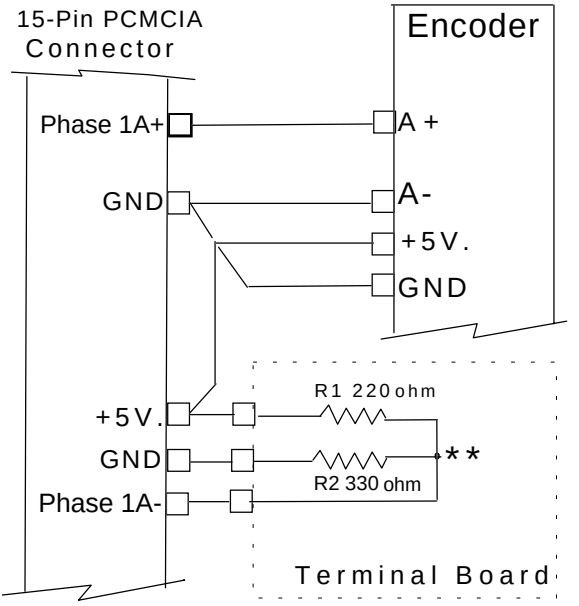

Figure 3-2. Single-Ended Configuration

** This resistor divider supplied by the user provides a bias voltage for the differential receiver. RES1 = 220 ohm resistor, RES2 = 330 ohm resistor (1/2-watt).

4.0 PROGRAMMING & OPERATION

4.1 Overview

The following section contains the commands to program the PCM-QUAD02 at the register level to accomplish a variety of functions. The heart of the PCM-QUAD02 is the LSI/CSI LS7266R1, a highly integrated component which reduces the need for external components. As seen in the LS7266R1 block diagram, many functions are controlled through register programming.

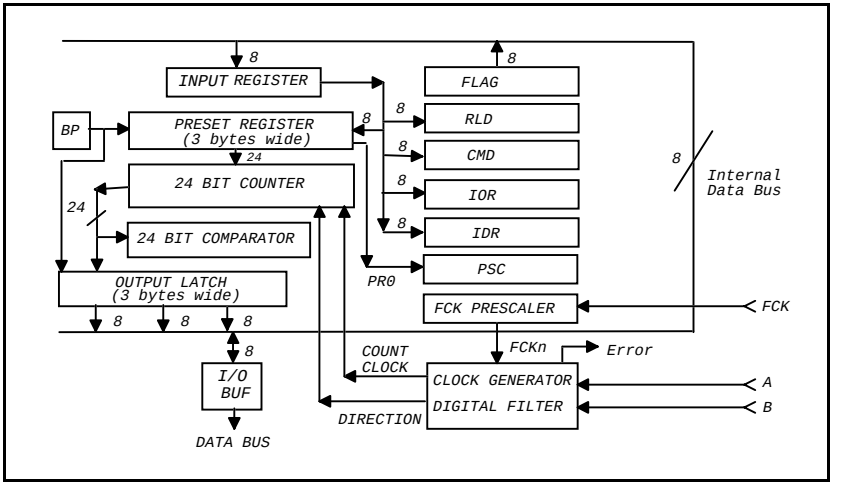

Figure 4-1. Block Diagram of LS7266R1 (One Channel)

For further details refer to the LS7266R1 data sheet.

4.2 Register Programming

As previously described, the LSI/CSI LS7266 is a highly integrated part requiring few external components. Most functions are controlled by programming registers in the LS7266. See attached LS7266 data sheet for further details.

v **Preset Registers - PR:**

Width is 24 bits, written to one byte at a time in sequence of three data write cycles.

v **Counters - CNTR:**

Counters are 24-bit synchronous, up/down, with clocks derived from A/B input. Counters are loaded with content of the PR registers.

v **Output Latches - OL:**

Data from each CNTR is derived from its associated OL and then read back on the data bus one byte at time in a sequence of three data read cycles.

v **Byte Pointers - BP:**

The bytes of the PR and OL are accessed one at a time, pointed to by the BP's, which are automatically incremented to address the next byte.

v **Filter Clock Prescalers - PSC:**

Each PSC is an 8-bit programmable modulo-N down counter driven by the FCK clock and allows independent filter clock frequencies for each channel. Factor N is loaded from the PR low byte register PR0.
Final Filter Clock frequency = Fck/(n+1)

v **Flag Register - FLAG:**

The FLAG register is the status register of the CNTR's.

Data Bit	Function
D0	BT: Borrow toggle flip-flop - toggles when CNTR underflows.
D1	CT: Carry toggle flip-flop - toggles when CNTR overflows.
D2	CPT: Compare toggle flip-flop - toggles when PR equals CNTR.
D3	S: Sign flag - 1 when CNTR underflows, 0 when CNTR overflows.
D4	E: Error flag - 1 when excessive noise at count inputs in quadrature mode.
D5	U/D*: Up/Down flag - 1 when counting up, 0 when counting down
D6	IDX: Index - 1 when selected index input is at active level.
D7	Not Used - always = 0.

v **Reset and Load Signal Decoders - RLD:**

Data Bit	Setting	Function
D0	0	NOP
	1	Reset BP
D1, D2	0, 0	NOP
	1, 0	Reset CNTR
	0, 1	Reset BT, CT, CPT, S
	1, 1	Reset E
D3, D4	0,0	NOP
	1,0	Transfer PR to CNTR (24 bits in parallel)
	0,1	Transfer CNTR to OL (24 bits in parallel)
	1,1	Transfer PR0 to PSC
D5, D6	0,0	Select RLD
D7	0	Select RLD addressed by X*/Y input
	1	Select both Channels RLD (override X*/Y input)

v **Counter Mode Registers - CMR:**

The functional modes of the programmable input and output pins.

Data Bit	Setting	Function
D0	0	Binary Count
	1	BCD Count
D1, D2	0,0	Normal Count
	1,0	Range Count
	0,1	Non-recycle Count
	1,1	Modulo-N Count
D3, D4	0,0	Non-quadrature
	1,0	Quadrature X1
	0,1	Quadrature X2
	1,1	Quadrature X4
D5, D6	1,0	Select CMR
D7	0	Select CMR addressed by X*/Y input
	1	Select both Channels CMR (override X*/Y input)

4.3 Mode Definitions:

Range Limit: An upper limit, set by PR, and a lower limit, set to 0, are set. The CNTR stops at CNTR=PR when counting UP, and CNTR=0 when counting DOWN. Counting resumes only when the count direction is reversed.
Non-Recycle: CNTR is disabled whenever overflow or underflow happens. End-of-cycle marked by Carry (UP) or Borrow (DOWN). Re-enabled by reset or load on CNTR.
Modulo-N: Count boundary set between 0 and content of PR. When counting up, at CNTR=PR, the CNTR is reset to 0 and the up-count is continued from that point. When counting down, at CNTR=0, the CNTR is loaded with content of PR and down-count is continued from that point.

Input/Output Control Registers - IOR:

The functional modes of the programmable input and output pins are as follows:

Data Bit	Setting	Function
D0	0	Disable inputs A and B
	1	Enable inputs A and B
D1	0	LCNTR/LOL pin Load CNTR input
	1	LCNTR/LOL pin Load OL input
D2	0	RCNTR/ABG pin is Reset CNTR input
	1	RCNTR/ABG pin is A and B Enable Gate input
D3, D4	0,0	CY is Carry output; BW is Borrow output (low)
	1,0	CY is Compare output; BW=Borrow output (low)
	0,1	CY is Carry/Borrow output (active low); BW is CPT (Compare toggle) output
	1,1	CY is CT (Carry toggle) output; BW is BT (Borrow toggle) output
D5, D6	0,1	Select IOR
D7	0	Select IOR addressed by X*/Y input
	1	Select both Channels IOR (override X*/Y input)

Index Control Registers - IDR:

Either LCNTR/LOL or RCNTR/ABG can be initialized to operate as an index input.

Data Bit	Setting	Function
D0	0	Disable Index
	1	Enable Index
D1	0	Negative Index Polarity
	1	Positive Index Polarity

D2	0	LCNTR/LOL pin is indexed
	1	RCNTR/ABG pin is indexed
D3, D4		Not Used
D5, D6	1	Select IDR
D7	0	Select IDR addressed by X*/Y input
	1	Select both Channels IDR (override X*/Y input)

The following registers are the Input Configuration Control and Interrupt registers.

Input Configuration Control:
Sets the routing for the Index (INDxSEL), counter cascading (PH2xSEL), and Carry/Borrow interrupt control (INTxSEL) signals.

Data Bit	**Setting**	**Function**
D0 - IND1SEL	0	Index 1 connected to Load Counter/Load Output Latch
	1	Index 1 linked to Reset Counter/Count Gate
D1 - IND2SEL	0	Index 2 connected to Load Counter/Load Output Latch
	1	Index 2 linked to Reset Counter/Count Gate
D2 - PH2BSEL	0	Counter 1 Phase B connected to Counter 2 Phase B input
	1	Counter 2 Phase B connected to Counter 2 Phase B input
D3 - PH2ASEL	0	Counter 1 Carry connected to Counter 2 Phase A input
	1	Counter 2 Phase A connected to Counter 2 Phase A input
D4 - INT1SEL	0	Disables Counter 1 Borrow to Interrupt - allows Carry to be configured as Compare to generate interrupt
	1	Combines Counter 1 Borrow/Carry (OR'd) for interrupt
D5 - INT2SEL	0	Disables Counter 2 Borrow to Interrupt - allows Carry to be configured as Compare to generate interrupt
	1	Combines Counter 2 Borrow/Carry (OR'd) for interrupt
D6,D7		Not Used

Interrupt Control:
To determine interrupt source and enable all interrupts (INTE), 0 = no interrupt from that source, 1 = interrupt generated. Interrupt is cleared by Write to Base + 6 register.

Data Bit	Function
D0 - CB1	Carry/Borrow 1 interrupt source
D1 - CB2	Carry/Borrow 2 interrupt source
D2 - IND1	Index 1 interrupt source
D3 - IND2	Index 2 interrupt source
D4 - INTE	Interrupts Enabled (= 1), Disabled (= 0)
D5, D6, D7	Not Used

Interrupt Mask:

Masks the interrupt source by setting = 0, enabling the interrupt = 1.

Data Bit	Function
D0 - M0	Mask (= 0) Carry/Borrow 1 interrupt
D1 - M1	Mask (= 0) Carry/Borrow 2 interrupt
D2 - M2	Mask (= 0) Index 1 interrupt
D3 - M3	Mask (= 0) Index 2 interrupt
D4-7	Not Used

*NOTE: If either or both of the Index pins are not used, they should be tied to ground and masked off to allow proper operation of the interrupt circuit.

4.4 Programming Examples

1. For two 24-bit non-quadrature counters, set the following registers and input either a single-ended or differential pulse source into A, with B controlling direction (Up = 1, Down =0):

Base + 4:	00x
RLD:	00x
CMR:	20x
IOR:	47x
IDR:	60x

2. For one 48-bit non-quadrature counter, change Base + 4 to 0Cx (this routes the signals correctly) and IOR to 57x (this makes the CY (Carry) output pin operate as the Carry/Borrow function).

3. For encoder input, x4 counting (no index functionality):

Base + 4:	00x (to use RCNTR/ABG input)
	03x (to use LCNTR/LOL input)
RLD:	00x
CMR:	38x
IOR:	47x
IDR:	60x

4. For encoder input, x1 counting, non-synchronous latching input on index (the output latch is set to the counter value when the index signal occurs (goes high)):

Base + 4:	03x
RLD:	00x
CMR:	28x
IOR:	43x
IDR:	60x

5. For encoder input, x1 counting, synchronous counter reset on index (that is, the counter is reset when the index signal occurs):

Base + 4:	00x
RLD:	00x
CMR:	28x
IOR:	43x
IDR:	65x

6. To load a counter, set three bytes; output them consecutively to the Preset Register, and transfer the Preset Register to the counter.

i.e., hibyte = 12x
midbyte = 34x
lobyte = 56x

```
Counter 0
output lobyte to Base + 0
output midbyte to Base + 0          'Byte Pointer gets
                                    incremented automatically
output hibyte to Base + 0
output 8 to Base + 1                'this transfers Preset Register to
                                    the counter
```

Now, prior to running the counter, reset the Byte Pointer and status flip-flops

```
output 5 to Base + 1
```

To read the count at any time, first transfer the counter to the Output Latch and then three consecutive reads will get the counter value.

```
output 10x to Base + 1              'this transfers counter to Output Latch
lobyte = input Base + 0             'Byte Pointer gets incremented
                                    automatically
midbyte = input Base + 0
hibyte = input Base + 0
                                    'now put the result together:
counter_value = 65536 * hibyte + 256 * midbyte + lobyte
```

7. Interrupt example: Use Channel 2 Index input to generate an interrupt and latch the counter value which can then be read using an ISR. (If Channel 1 not used or Index not connected, remember to mask it off).

```
RLD:                03x     'reset Byte Pointer and Counter
RLD:                04x     'reset BT,CT,CPT,S
CMR:                28x     'see LS7266 spec
IOR:                43x     'see LS7266 spec
IDR:                63x     'see LS7266 spec
output Base + 4:    02x     'Route Channel 2 Index to LCNTR/LOL
output Base + 6:    10x     'Enable interrupts
output Base + 7:    08x     'Mask Channel 2 Index
                            'Now when the Index pulse occurs, an
                            interrupt will be generated and the
                            counter value will be latched
ISR:                        Read the counter value and perform
                            other tasks
output Base + 6     10x     'Clears the interrupt while keeping
                            interrupts enabled
```

4.5 Interrupt Control

As mentioned earlier, the interrupts and Index Carry/Borrow are routed to the FPGA which passes it to the PCMCIA bus interrupt signal. Card and Socket Services has determined which interrupt to pass through to the PC (IRQ's 0 to 15 can be used as given in the CIS). Through the Interrupt Control registers, the interrupt function can be disabled and individual interrupts can be masked off. The signal generating the interrupt is determined by reading the Interrupt Status register. The interrupts generated are Level Mode only.

5.0 SPECIFICATIONS

Typical for 25°C unless otherwise specified.

Power consumption

(Not supplying power to external encoders)

+5V	80 mA max, 50 mA typical

(Typical supplying 1 Dynamics Research Incremental Optical Rotary Encoder part number M21AAFOBB2E-2500)

+5V	179 mA
Max. peak current to encoders (each)	400 mA

Input Section

Receiver type	SN75ALS175 quad differential receiver
Configuration	Each channel consists of PhaseA input, PhaseB input and Index input; each configured for differential input
Number of channels	2
Common mode input voltage range	±12V max
Differential input voltage range	±12V max
Input sensitivity	±200mV
Input hysteresis	50mV typ.
Input impedance	12 kohm min.
Propagation delay	27 ns max.
Absolute maximum input voltage	
Differential	±25V max.
Miscellaneous	Meets EIA RS422, 423, 485 and CCITT V.10, V.11, X.26, X.27. Designed for Multipoint busses on long lines in noisy environments.

Counter Section

Counter type	LS7266R1 24-bit Dual-axis Quadrature Counter
Quadrature Mode	
Clock frequency	4.3 MHz max
Separation	57 ns min
Clock pulse width	115 ns min
Index pulse width	85 ns min
Count Mode	
Clock frequency	30 MHz max, (25 MHz max Mod-N mode)
Clock A - high pulse width	16 ns min
Clock A - low pulse width	16 ns min
Filter clock (FCK)	10 MHz
Digital filter rate	10 MHz, software-selectable divider (1 to 256 in single steps)
Crystal oscillator (FCK source)	
Frequency	10 MHz
Frequency accuracy	100 ppm

Interrupt Controller Section

Controller type	FPGA
Configuration	Polled mode only
Interrupts	2 to 15
Interrupt enable	Programmable
Interrupt sources	All Carry/Borrow outputs from LS7266R1, all Index inputs

Environmental

Operating temperature range	0 to 70°C
Storage temperature range	–40 to 100°C
Humidity	0 to 90% non-condensing

For your notes.

For your notes.

EC DECLARATION OF CONFORMITY

We, Measurement Computing Corporation, declare under sole responsibility that the product:

Part Number	Description
PCM-QUAD02	Incremental quadrature encoder PCMCIA cards

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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